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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 1400.1374040

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on February 23, 2007

Signature: /Ross D Snyder/

Typed or printed name: Ross D. Snyder, Reg No 37730

Application Number	Filed
10/691,137	10-22-2003

First Named Inventor: Robert Elliott Robotham

Art Unit	Examiner
2188	McFadden, M B

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [ ] attorney or agent of record. Registration number _____
- [X] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34: 37,730

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02-23-2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Robert Elliott Robotham

Title: METHOD AND APPARATUS FOR ACCESSING DATA SEGMENTS HAVING ARBITRARY ALIGNMENT WITH THE MEMORY STRUCTURE IN WHICH THEY ARE STORED

App. No.: 10/691,137 Filed: 10-22-2003

Examiner: McFadden, Michael B Group Art Unit: 2188

Atty. Dkt. No. 1400.1374040

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Claims 1-20 are pending in this application. The Examiner has allowed claims 1-5. Claims 6-19 are rejected and claim 20 is objected to by the Examiner. Appellant respectfully requests reconsideration of pending claims 1-20. Appellant files herewith a notice of appeal. Pursuant to the "New Pre-Appeal Brief Conference Pilot Program," 1296 Off. Gaz. Pat. Office 67 (July 12, 2005) and the "Extension of the Pilot Pre-Appeal Brief Conference Program" dated 1/10/2006, Appellant submits a pre-appeal brief request for review. The review is requested for the reasons set forth below:

Applicant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection. Applicant submits the Examiner's "Response to Arguments" provides evidence that the Examiner has failed to consider the pending claims as required by the Manual of Patent Examining Procedure (MPEP) and prevailing case law. For anticipation under 35 U.S.C. § 102, a reference must teach every aspect of the claimed invention either explicitly or implicitly. Any feature not directly taught must be inherently present [emphasis added]. See MPEP 706.02 – distinction between 35 U.S.C. § 102 and § 103. As Applicant describes in detail below, Applicant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection. Furthermore, MPEP § 2141 sets forth the Graham inquiries for a rejection under 35 U.S.C. § 103. MPEP § 2143 describes basic requirements of a *prima facie* case of obviousness under 35 U.S.C. § 103. As Appellant describes in detail below, Appellant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection.

The Examiner has rejected claims 6, 7, 10, 11, 14, and 18 under 35 U.S.C. § 102(b) as being anticipated by Ukai et al. (U.S. Patent No. 5,809,516). Regarding claims 6 and 10, Applicant submits, as one example, the cited portion of the cited reference fails to disclose "...a second portion of the plurality of storage devices is accessed at a second hardware memory address adjacent to the first hardware memory address" and "...the second hardware memory address being adjacent to the first hardware memory address." While the Examiner cites "column 29, lines 53-56," Applicant notes the context within which such lines appear. For example, Applicant notes column 29, lines 56-61, state, "As illustrated, the first write request to the logical unit #U0 is allocated the physical block (#L0) in the logical unit #U0; the first write request to the logical unit #U1 is allocated the physical block (#L7) in the logical unit #U1 because the physical block #L7 meets the condition of step 454." Also, the Examiner states, "The reference show a RAID Level 5 disc array that shows the logical blocks of memory are allocated adjacent to each other and are accessed concurrently (in parallel)." However, the Examiner cites "Figure 38 and column 29, lines 53-56,"of the cited reference as allegedly disclosing such purported teaching. Yet, column 29, lines 53-56, of the cited reference merely state, "The numbers in FIG. 38 constitute the sequence in which the corresponding logical blocks are allocated to the physical blocks in the same logical unit." While the cited portion of the cited reference refers to a "sequence," the Examiner, to the contrary, alleges such teaching "...shows the logical blocks of memory are...accessed concurrently (in parallel)." Applicant submits the teaching of the cited portion of the cited reference fails to support the Examiner's purported interpretation of such teaching. Also, the Examiner states, "However, the limitation of the claim states that the memory addresses are merely adjacent." Applicant submits the Examiner apparently fails to consider the word "hardware" in claims 6 and 11.

Regarding claims 7 and 11, Applicant submits, as one example, the cited portions of the cited reference fail to disclose "...with respectively separate address buses." The Examiner states, "Note that Figures 1, 18, 24, and 32 show that four drives are accessed separately using a different bus. Furthermore note that inherently, each bus includes an address control and data lines." Applicant does not see disclosure of the purported "a different bus" in the cited portion of the cited reference. Moreover, Applicant does not see disclosure of the "respectively separate address buses" in the cited portion of the cited reference. While the Examiner asserts a rejection based on inherency, Applicant submits that the teachings of the cited reference fail to establish inherency in accordance with existing law. For example, Applicant submits that the Examiner has failed to establish that the public gained the benefit of the subject matter recited in claim 7 from the teachings of the cited reference. *Schering Corp. v. Geneva Pharmaceuticals*, 339 F.3d 1373 (Fed. Cir. 2003). As another example, Applicant submits that the Examiner has failed to establish that the subject matter recited in claim 7 is present in the teachings of the cited reference. *Mentor v. Medical Device Alliance*, 244 F.3d 1365 (Fed. Cir. 2001); *Scaltech v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999). Thus, Applicant submits that the subject matter recited in claim 7 cannot be considered to be inherent in the teachings of the cited reference. Accordingly, Applicant

submits the Examiner has failed to satisfy the burden of proof required for asserting a rejection based on inherency.

Regarding claim 14, as one example, Applicant submits the cited portions of the cited reference fail to disclose "...accessible via a plurality of modes of access to allow selection among a plurality of predefined memory access starting points...." The Examiner cites "(column 4, lines 19-22 and column 4, lines 48-49)." However, Applicant notes such portions merely refer to "...different write requests may be executed in parallel..." and "A plurality of read requests are executed in parallel...." As another example, Applicant submits the cited portions of the cited reference fail to disclose "... wherein the predefined memory access starting points occur at intervals of less than a total memory bandwidth." The Examiner cites "(Figure 37 and column 4, lines 48-53)." However, Applicant notes Figure 37 relates to "LOGICAL BLOCK NUMBERS IN EACH LOGICAL UNIT" and column 4, lines 48-53, refers to "A plurality of read requests are executed in parallel..." and "...a maximum number of read requests that may be executed is equal to the maximum number of disc drives configured."

Regarding claim 19, Applicant submits, as one example, the cited portions of the cited reference fail to disclose "...wherein the amount of desired data is stored contiguously within a system memory address space of the memory system." The Examiner cites "(Figure 38 and column 29, lines 53-56)." However, Applicant notes Figure 38 relates to "LOGICAL BLOCK ALLOCATION SEQUENCE IN EACH LOGICAL UNIT" and does not appear to teach "...wherein the amount of desired data is stored contiguously within a system memory address space of the memory system."

The Examiner has rejected claims 8, 9, 12, 13, 17, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Ukai et al. ((U.S. Patent No. 5,809,516) hereinafter Ukai) as being applied to claims 6, 10, and 14 above, and further in view of Yokote et al. ((U.S. Patent No. 5,651,129) hereinafter Yokote). Regarding claims 8 and 12, as one example, Applicant submits the cited portions of the cited reference fail to disclose "...the larger storage device comprising an input to select an addressing mode." The Examiner cites "(Figure 2, element 24 and column 3, 24-32)." However, Applicant can find no mention of "...an input to select an addressing mode" in such cited portions. Moreover, the Examiner states, "At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai (Figure 1, element 4) with the controller/memory modules of Yokote (Figure 1, element 16). The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage (Yokote – column 1, lines 54-57)." However, given the historical differences in properties of "disk drives" and "controller/memory modules" (e.g., capacities), replacing the disk drives of Ukai with the controller/memory modules of Yokote could be expected to lower the storage capacity. Thus, Applicant submits one of ordinary skill in the art would not have been so motivated to combine the alleged teachings of the cited references.

Regarding claim 9, as one example, Applicant submits the cited portions of the cited reference fail to disclose "...wherein the addressing mode allows selection of different hardware memory addresses among the plurality of storage devices for a same memory access operation." The Examiner cites "(column 3, lines 24-32 and column 3, 48-54)." However, Applicant can find no mention of "...for a same memory access operation" in such cited portions. Moreover, the Examiner states, "At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai (Figure 1, element 4) with the controller/memory modules of Yokote (Figure 1, element 16). The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage (Yokote – column 1, lines 54-57)." However, given the historical differences in properties of "disk drives" and "controller/memory modules" (e.g., capacities), replacing the disk drives of Ukai with the controller/memory modules of Yokote could be expected to lower the storage capacity. Thus, Applicant submits one of ordinary skill in the art would not have been so motivated to combine the alleged teachings of the cited references.

Regarding claim 13, as one example, Applicant submits the cited portions of the cited reference fail to disclose "...wherein the addressing mode allows selection of different hardware memory addresses among the first storage device and the second storage device for a same memory access operation." The Examiner cites "(column 3, lines 24-32 and column 3, 48-54)." However, Applicant can find no mention of "...for a same memory access operation" in such cited portions. Moreover, the Examiner states, "At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai (Figure 1, element 4) with the controller/memory modules of Yokote (Figure 1, element 16). The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage (Yokote – column 1, lines 54-57)." However, given the historical differences in properties of "disk drives" and "controller/memory modules" (e.g., capacities), replacing the disk drives of Ukai with the controller/memory modules of Yokote could be expected to lower the storage capacity. Thus, Applicant submits one of ordinary skill in the art would not have been so motivated to combine the alleged teachings of the cited references.

Regarding claim 17, as one example, Applicant submits the cited portions of the cited reference fail to disclose "...wherein the predefined memory access starting points occur in the memory banks as a function of a size of a desired data block to be accessed." The Examiner cites "(Figure 2)" and "(Column 2, lines 50-62)." However, Applicant can find no reference to "predefined memory access starting points" occurring as recited in claim 17 within the cited portion of the cited reference. Moreover, the Examiner states, "At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai (Figure 1, element 4) with the controller/memory modules of Yokote (Figure 1, element 16). The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage (Yokote – column 1, lines 54-57)." However, given the historical differences in properties of "disk drives" and "controller/memory modules" (e.g., capacities), replacing the disk drives of Ukai with the controller/memory

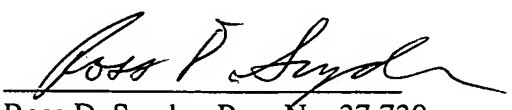
modules of Yokote could be expected to lower the storage capacity. Thus, Applicant submits one of ordinary skill in the art would not have been so motivated to combine the alleged teachings of the cited references. Accordingly, Applicant submits claim 17 is not rendered obvious, but is in condition for allowance.

Regarding claim 18, as one example, Applicant submits the cited portions of the cited reference fail to disclose "...wherein the amount of desired data is an asynchronous transfer mode (ATM) cell." The Examiner cites "(Figure 1, element 14 and Column 2, lines 59-62)." However, Applicant can find no reference to "...wherein the amount of desired data is an asynchronous transfer mode (ATM) cell" occurring as recited in claim 18 within the cited portion of the cited reference. Moreover, the Examiner states, "At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai (Figure 1, element 4) with the controller/memory modules of Yokote (Figure 1, element 16). The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage (Yokote – column 1, lines 54-57)." However, given the historical differences in properties of "disk drives" and "controller/memory modules" (e.g., capacities), replacing the disk drives of Ukai with the controller/memory modules of Yokote could be expected to lower the storage capacity. Thus, Applicant submits one of ordinary skill in the art would not have been so motivated to combine the alleged teachings of the cited references. Accordingly, Applicant submits claim 18 is not rendered obvious, but is in condition for allowance.

The Examiner has rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Ukai et al. ((U.S. Patent No. 5,809,516) hereinafter Ukai) as applied to claim 15 above, and further in view of Koutsoures (U.S. Patent No. 6,457,075). Applicant respectfully disagrees. Regarding claim 16, the Examiner alleges Koutsoures discloses the memory system of claim 15 wherein the total memory bandwidth is equal to the burst size, citing "(Column 2, lines 44-46)." While the cited portion of the cited reference refers to "cache line length," Applicant can find no teaching in the cited portion of the cited reference of the "cache line length" being "the total memory bandwidth."

Respectfully submitted,

02/23/2007
Date



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